REMARKS/ARGUMENTS

In an Office Action mailed July 28, 2004, the Examiner rejected claims 1-10 and 13-39. For the reasons set out below, Applicants respectfully request that the Examiner withdraw the rejections and allow claims 1-10 and 13-39.

In addition, applicants respectfully request that the Examiner enter and allow new claim 40. A Request for Continued Examination is filed herewith.

§ 112:

In the Office Action , the Examiner rejected claims 21, 26 and 31 under 35 USC § 112. Specifically, the Examiner rejected claims 21, 26 and 31 for an alleged lack of antecedent basis for the terms "the non-metal layer" (claims 21 and 26) and "the power conducting portion" (claim 31). The Examiner also rejected claim 31 as allegedly failing to particularly point out and distinctly claim the subject matter. Applicants respectfully submit that amended claims 21, 26 and 31 are not invalid under § 112 for lack of antecedent basis and that claim 31 is not invalid under § 112 for indefiniteness.

§ 102:

The Examiner rejected claims 1-10 and 13-39 as allegedly unpatentable over US 6,056,391 (Kasamoto) under 35 USC § 102. Applicants respectfully disagree. Applicants respectfully submit that the Examiner has not shown a prima facie case of anticipation at least because Kasamoto does not disclose each and every limitation of the rejected claims. In the discussion below, Applicants separate the reasons into two sections. In the first section, relating to all pending claims 1-10 and 13-39, Applicants discuss the allowability of the claims based on the failure of Kasamoto to disclose limitations relating to a "power bus" and/or "power via" (claims 1-10, 13-20 and 36-39) and/or "providing power to a resistor" (claims 21-30) and/or "connecting a power source to the top layer" (claims 31 and 32) and/or "a power supply portion" (claims 33-35).

In the second section, relating to pending claims 2, 13, 17-20, 36-39, Applicants discuss the allowability of claims based on the failure of Kasamot to disclose limitations relating to both a "power bus" and a "controller bus," and/or both a "power via and a controller via" (claims 2, 8, 13, 17-20), and or both a "power bus" and a "FET bus" (claims 36-39).

Claims 1-10 and 13-39:

Applicants respectfully submit that claims 1-10 and 13-39 are not invalid as anticipated by Kasamoto at least because Kasamoto does not disclose each and every limitation of the rejected claims. For example, Kasamoto does not disclose at least the following limitations:

> ". . . the second metal layer comprises a separation barrier located adjacent the first metal layer and between at least one resistor of the plural resistors and the power bus."

claim 1 and dependent claims 2-9;

> " . . . connecting a power bus to the at least one thin film resistor with a power via . . . ."

independent claim 10 and dependent claims 13-16;

> " . . . creating a separation barrier to substantially prevent spreading of ink corrosion from the resistors to the power bus and the controller bus . . . ."

independent claim 17 and dependent claims 18-20;

> " . . . a first metal layer comprising a portion for providing power to a resistor . . . wherein the first metal layer is electrically connected to the electrical connection portion of the bottom layer portion at the via."

independent claim 21 and dependent claims 22-30;

> " . . . a bottom metal layer for connecting a power source to the top metal layer, wherein the bottom metal layer is electrically connected to the top metal layer at the electrical connection portion and the electrical connection portion comprises a corrosion barrier between bottom metal layer and the top conductive layer portion."

independent claim 31 and dependent claim 32;

> " . . .a first conductive metal layer comprising a power supply portion for providing a common supply of electrical power to the plurality of resistors;
>
> a second metal layer comprising a top conductive layer portion and a bottom layer portion, wherein the bottom layer portion comprises the plurality of resistors and a plurality of electrical connection portions corresponding to the plurality of resistors, wherein the second metal layer is connected to the first conductive metal layer portion at the plurality of electrical connection portions."

independent claim 33 and dependent claims 34 and 35;

> " . . . providing a first metal layer comprising a power bus and a FET bus . . . ."

independent claim 36 and dependent claims 37-39. All of the rejected claims include additional limitations that further distinguish each claim over Kasamoto.

In support of the rejections, the Examiner states that Kasamoto discloses: "a first/bottom metal layer (FIG. 1c, element 1110c-b) comprising a power bus/conductive trace coupled to the power source . . . ." Applicants respectfully disagree.

In Kasamoto, the "common lead electrode layer structure including an upper electrode layer 1110c and a lower electrode layer 1110b" is not disclosed as being a power bus and is not "a portion for providing power to a resistor" as recited, for example, in claim 21. As shown in FIG. 1A, the upper electrode

layer 1110c of the common lead electrode layer structure is the "return portions of the electrodes" which are "made common as a wide conductive layer . . . ." 6:62-65; 1:53-58; FIGS. 1A-1C.

Kasamoto does not disclose, for example, "connecting a power bus to the at least one thin film resistor with a power via" as recited in claim 10 or "a first metal layer comprising a portion for providing power to a resistor . . . wherein the first metal layer is electrically connected to the electrical connection portion of the bottom layer portion at the via" as recited in claim 21. For similar reasons, Kasamoto does not disclose all of the limitations of any of the pending claims. For example, Kasamoto does not disclose at least those limitations set out above.

In support of the rejection, the Examiner stated that "Kasomoto's disclosure solves the problem of ink permeates through the step portion at vias and causes electrical corrosion, resulting in the disconnection of the resistor." Page 5, first full paragraph (citing 2:35-45). Applicants respectfully submit that this statement does not support a rejection of the claims because it does not address the claim language. Moreover, Kasamoto does not state that "ink permeates through the step portion at vias" as stated by the Examiner. Kasamoto discusses that "ink permeates through the step portion and causes electric corrosion . . . ."

Claims 2, 13, 17-20, 36-39:

Applicants respectfully submit that claims 13, 17-20 and 36-39 are not anticipated by Kasamoto at least because Kasamoto does not disclose each and every limitation of the rejected claims. For example, Kasamoto does not disclose at least the following limitations in the claimed combinations:

> " . . . a power bus . . . and at least one power via . . . [(claim 1) and] further comprising a controller bus that is connected to the at least one resistor at a controller via . . . ."

claim 2;

> " . . . connecting a power bus to the at least one thin film resistor with a power via [(claim 10) and] further comprising routing power from the at least one thin film resistor to at least one controller via."

claim 13;

> " . . . creating conductive trace routes from the power bus to power vias associated with each resistor . . . and from the controller bus to controller vias associated with each resistor"

independent claim 17 and dependent claims 18-20;

> " . . . providing a first electrical connection between the power bus and the second metal layer and a second electrical connection between the second metal layer and the FET bus, wherein the first and second electrical connections are made through the corrosion-resistant layer portion."

independent claim 36 and dependent claims 37-39. All of the rejected claims include additional limitations that further distinguish the claims over Kasamoto.

In support of the rejection, the Examiner stated that, Kasamoto also allegedly discloses "a controller/FET bus that is connected to the at least one resistor at a controller via (FIG. 1C: A corresponding connection connects the electrode 1110a to a power controller)." Applicants respectfully do not understand where in Kasamoto the Examiner finds support for this assertion. In FIG. 1A, the resistors 1103 are shown associated with only one through-hole 1105 each.

Kasamoto FIG. 1C purports to show a "through-hole 1105" where a "resistor layer 1103" meets an "upper electrode layer 1110c" where the "common lead electrode layer structure including an upper electrode layer 1110c and a

lower electrode layer 1110b." Kasamoto also states that the common lead electrode layer structure is the "return portions of the electrodes" which are "made common as a wide conductive layer . . . ." 6:62-65; 1:53-58; FIGS. 1A-1C. Kasamoto does not disclose both a "power via" and a "controller via" as recited in claims 2 and 13, does not disclose both "creating conductive trace routes from the power bus to power vias associated with each resistor . . . and from the controller bus to controller vias associated with each resistor" as recited in claim 17 and does not disclose "providing a first metal layer comprising a power bus and a FET bus" as recited in claim 36.

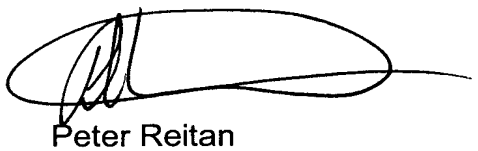
New Claim 40:

Applicants respectfully request that the Examiner enter and allow new claim 40. New claim 40 is supported in the Specification at least at FIGS. 4 and 5 and page 8, line 26 through page 9, line 12.

CONCLUSION

For reasons set out above, Applicants respectfully request that the Examiner withdraw the rejections to claims 1-10 and 13-39 and allow claims 1-10 and 13-40.

Respectfully submitted,



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